What is claimed is:

1. A chip scale package comprising:

a plurality of terminals for making external electrical connections;

a chip having a plurality of bonding pads on an active surface thereof, the bonding pads electrically connected to the terminals, wherein a backside surface of the chip is exposed from a surface of the chip scale package; and

an ink mark formed on the backside surface of the chip.

2. A method for marking wafer-level chip scale packages, the method comprising the following steps:

providing a wafer having a plurality of dice formed thereon, wherein the dice have been packaged into a plurality of semi-finished chip scale packages, wherein the semi-finished chip scale packages comprises a plurality of terminals for making external electrical connections, each die has a plurality of bonding pads on an active surface thereof, the bonding pads are electrically connected to the terminals, and a backside surface of each die is exposed from a surface of the semi-finished chip scale packages;

positioning the semi-finished chip scale packages formed on the wafer;

printing ink marks on the exposed backside surface of the dice;

curing the ink marks on the dice; and

dicing the wafer to obtain a plurality of chip scale packages wherein each package is separated from other packages.

3. The method as claimed in claim 2, further comprising a step of removing defective ink marks after the printing step and before the curing step.

4. The method as claimed in claim 2, wherein the positioning step is performed by a positioning device and the printing step is performed by a printing device, the positioning device and the printing device are positioned on two opposing sides of the wafer, and the printing step is performed by coaxially aligning the printing device with the positioning device.

5. The method as claimed in claim 2, wherein the wafer has a plurality of dicing streets between the semi-finished chip scale packages, and the position step is performed by

finding the dicing street with a charge coupled device (CCD).

6. The method as claimed in claim 5, wherein the positioning step is performed by a positioning device and the printing step is performed by a printing device, the positioning device and the printing device are positioned on two opposing sides of the wafer, and the printing step is performed by coaxially aligning the printing device with the positioning device.

7. A semiconductor wafer comprising a plurality of dice wherein each of dice has a plurality of bonding pads on an active surface thereof and an ink mark on a backside surface thereof.

8. A semiconductor die comprising a plurality of bonding pads on an active surface thereof and an ink mark on a backside surface thereof.